REMARKS

Favorable reconsideration of this application in light of the following remarks is respectfully requested.

Claims 1-6 and 13 are pending within this application. Claims 7-12 are canceled herein. Claim 1 is amended herein. Claim 13 is newly added herein. No claims have been allowed.

Election/Restriction

Applicant notes applicant's election/restriction within paper 4.

Claim Objections —35 U.S.C. § 112

The Examiner has objected to claim 1 incident to an informality therein. In response, applicant has amended claim 1 accordingly, to address the informality therein.

In light of the foregoing response, applicant respectfully requests that the Examiner's objection to applicant's claim 1 be withdrawn.

Claim Rejections -- 35 U.S.C. § 102

The Examiner has rejected claims 1-6 under 35 U.S.C. § 102(e) as being anticipated by Wang et al. (U.S. Pub. No. 20020155672 A1; hereinafter "Wang").

In response, applicant has: (1) amended claim 1 to incorporate therein the limitations of claim 5, while canceling claim 5; and (2) added new claim 13 which derives from claim 1 and claim 4, to provide within amended claim 1 and newly added claim 13 subject matter which applicant believes to patentably distinguish applicant's invention as disclosed and claimed therein from that which is disclosed within Wang.

In that regard, applicant has amended claim 1 to provide that applicant's at least one fuse layer and the highest of applicant's series of patterned conductor layers are formed of different conductor materials. In addition, applicant has provided within claim 13 that applicant's at least one fuse layer is formed simultaneously with an alignment mark within the microelectronic fabrication.

In comparison, Wang's bond pad 112b and series of patterned conductor layers 112b are formed of the same conductor material incident to patterning from Wang's blanket conductor layer 112. Further, Wang does not apparently within Wang's disclosure disclose an alignment mark, and applicant does not believe that Wang's bond pad 112b may be considered an alignment mark. In particular, applicant notes that while the Examiner asserts that Wang's passivation layer is etched and aligned with a bond pad to form an alignment mark, applicant's invention as disclosed within Fig. 3 and Fig. 4 provides for an alignment mark that is formed employing a planarizing process rather than a etching process.

Thus, since each and every limitation within applicant's invention as disclosed and claimed within amended claim 1 and claim 13 is not disclosed within Wang, in particular with respect to: (1) a patterned conductor layer and a fuse being formed of different materials; and (2) a fuse formed simultaneously with an alignment mark within a microelectronic fabrication, applicant asserts that amended claim 1 and newly added claim 13 may not properly be rejected under 35 U.S.C. § 102(e) as being unpatentable over Wang. Since all remaining claims within the foregoing rejection are dependent upon amended claim 1 and carry all of the limitations of amended claim 1, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(e) as being anticipated by Wang.

In light of the foregoing response, applicant respectfully requests that the Examiner's rejections of claims 1-6 under 35 U.S.C. § 102(e) as being unpatentable over Wang be withdrawn.

Other Considerations

Applicant notes the additional prior art of record cited by the Examiner but not employed in rejecting applicant's claims to applicant's invention, in particular: (1) Barth et al. (U.S. Patent No. 6,559,042); (2) Tottori (U.S. Pub. No. 2002/0014680); (3) Ema (U.S. Patent No. 5,297,541); and (4) Tzeng et al. (U.S. Patent No. 6,180,503) as generally pertinent to applicant's invention. No fee is due as a result of this amendment and response.

SUMMARY

Applicant's invention as disclosed and claimed within amended claim 1 and claim 13 is directed towards a method for fabricating a microelectronic fabrication having formed therein a patterned conductor layer and a fuse layer. Within applicant's invention, the fuse layer is formed at a level no lower than a highest of the series of patterned conductor layers. Within one aspect of the invention, the at least one fuse layer and the highest of the series of patterned conductor layers are formed of different conductor materials. Within another aspect of the invention, the at least one fuse layer is formed simultaneously with an alignment mark within the microelectronic fabrication. Absent from the prior art of record employed in rejecting applicant's claims to applicant's invention is a disclosure of each and every limitation within applicant's invention.

CONCLUSION

On the basis of the above remarks, reconsideration of this application, and its early allowance, are respectfully requested. Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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